Navneet

Senior Undergraduate, Department of Electrical Engineering, IIT Bombay, India
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Education

Indian Institute of Technology Bombay **[2020 - Present]**
Bachelor of Technology with Honors in Electrical Engineering; **GPA: 9.05/10**

Publications and Conferences

- **Navneet**, Anubhav Bhatla, Biswabandan Panda **"The Maya Cache: A Storage-efficient and Secure Fully-associative Last-level Cache"**, *51st International Symposium on Computer Architecture (ISCA 2024)* (under review)
- Secured **2nd** position for successful demonstration of **SANKET (Antenna Deployment System)** at the International Conference for Small Satellites, India, 2022

Academic Achievements & Honours

- Awarded **Undergraduate Research Award** for my remarkable research on **Secure Last Level Cache** [2023]
- Awarded **Best Project Award** for building **Hazardous Gas Detection bot with VSLAM** [2023]
- Conferred with **KVPY (Young Scientist Incentive Plan)** fellowship with an All-India Rank **191** out of nearly 50,000 students in **SA-stream**, organised by **Indian Institute of Science, Bangalore** [2019]
- Achieved All-India Rank **649** out of 1,170,000 participants in **JEE (Main) 2020** [2020]
- Awarded **Certificate of Merit** in **NSEA** and **NSEJS** (National Standard Examination in Astronomy and Junior Science) for having been among **Top 1%** students among **53900+** candidates, organized by **IAPT** [2019, 2018]

Research Experience

Storage-efficient and Secure Fully-associative Last-level Cache **[May '21 - Jul '22]**
Guides: *Prof. Biswabandan Panda, Computer Science, IIT Bombay*
- Proposed a secure and storage-efficient **shared LLC** to mitigate eviction-based **side-channel attacks**
- The design incorporates a decoupled tag and data store in the LLC, utilizing pointer-based indirection for 0% storage overhead compared to the non-secure baseline LLC, with minimal performance impact
- Idea is motivated by **Reuse** cache and **Mirage** cache which allowed us to reduce the size of the data store and keep the security similar to **Mirage** without hurting the performance too much

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Shared Translation Lookaside Buffer Prefetching **[Aug '23 - Present]**
Guide: Prof. Virendra Singh, Computer Science and Engineering, IIT Bombay
- Performed literature survey on various **TLB(Translation Lookaside Buffer)**, data and instruction **prefetchers**
- Designed prefetchers in **Champsim** in pursuit of a single prefetcher for instruction and data-related translations
- Performed extensive tests using the **SPEC** benchmark suite and server workloads
  Future Work: Exploit on-chip **Branch-Predictor** to issue **STLB** prefetches for both data and instruction-related translation depending on the predicted control path which could result in reduced area overhead

Internships

Texas Instruments | Digital Systems Intern **[May '23 - Jul '23]**
A global semiconductor company aims to design and manufacture analog and embedded processing chips.
- Performed extensive analysis of interrupt signals of **RADAR SOC** built for automobile application
- Developed verilog logic for interrupt signals to detect **pulse-triggered** or **level-triggered** behaviour
- Designed a flow using **SystemVerilog Assertion** to detect any anomaly in the early stages of design and testing
- Integrated an automated process using **Python** and **SystemVerilog** in the main development pipeline that monitors and generates the status for all interrupt signals

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NanoSniff Technologies | Embedded Systems Intern **[Dec '21 - Jan '21]**
A MEMS Fabrication and R&D company to productize the technology in the field of nanoelectronics
- Developed a solar-powered wireless data acquisition system using two **ESP32 wroom** module
- Designed charging circuit for Li-ion batteries using a dynamic power path management system with solar panels for uninterrupted power supply for a remote ESP32 node
- Created a **Python GUI** to collect data from the remote esp32 node and maintain a database using **PostgreSQL**

Technical Projects

Hazardous Gas detection using Nanosaur with VSLAM **[Jan '23 - Apr '23]**

Guide: Prof. Siddarth Tallur, Electrical Engineering, IIT Bombay

- Designed an electronic circuit with gas sensors to detect gases like NH3, CO2, CO, CH4, etc., and integrated it with **Nvidia Jetson Nano**
- Implemented a VSLAM technique; **ORBSLAM-2** with a stereo camera on jetson nano
- Integrated the sensor system and the **ORBSLAM-2** with a **Jetson Nano** based robot, Nanosaur, using **ROS2**
- Established remote control with the robot over wifi and set up a local server-based dashboard to collect gas intensity levels and show the 3D map of the environment

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Hardware design for SANKET(Antenna Deployment System) **[May '21 - Aug'23]**

Student Satellite Program | IIT Bombay (Website)

- Developed **embedded C** code for the **Atmega128** microcontroller to control an antenna deployment system
- Successfully performed system-level integration and testing of various components, including current limiters and voltage regulators, along with **Atmega128** for antenna deployment
- Designed **RF PCB** to mount antennas with **impedance matching** techniques to ensure optimal transmission

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Fault Tolerant Core using FXA Architecture **[Aug '23 - Dec '23]**

Guide: Prof. Virendra Singh, Computer Science and Engineering, IIT Bombay

- Modelled **REMO**, a fault-tolerant core in **GEM5** using an in-order verifier for each instruction
- Modified the existing flow to model **FXA** architecture along with REMO fault tolerant feature
- Performed extensive testing and evaluated impact on performance using **SPEC06** benchmark suite

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Design and Simulation of an Out-of-Order Superscalar Processor **[Sep '22 - Jan '23]**

Guide: Prof. Virendra Singh, Computer Science and Engineering, IIT Bombay

- Coordinated a four-member team to design a **2 way fetch superscalar Out-of-Order Processor**
- Designed logic for 2-bit branch predictor, Fetch, Decode, Reservation station, ROB along with register renaming
- Implemented the complete design of the processors and **tested** it on **VHDL** using **Quartus Prime**

Image Deblurring using Image Deconvolution | Course Project **[Feb '23 - Apr '23]**

Guide: Prof. Amit Sethi, Electrical Engineering, IIT Bombay

- Leveraged **Deep CNN** to restore blurred images, effectively reversing the effects of motion blur
- Utilized **transfer learning** to improve model performance, remove noise, minimize unwanted artifacts and accelerate convergence by fine-tuning the **pre-trained CNN** on a dataset of 12240 image patches
- Achieved a significant reduction in unwanted artifacts while improving the image deblurring accuracy up to **92%** by employing the deep learning model built using **tensorflow** in python

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System Design with Microprocessor | Microprocessor Lab **[Jan '22 - Apr '22]**

Guide: Prof. Saravanan Vijaykumaran, Electrical Engineering, IIT Bombay

- Implemented **binary search** algorithm in **assembly** language on **8051** microcontroller
- Developed embedded C codes for **8051**to interface peripheral using a serial protocol like **UART** and **SPI**
- Developed an interface of an **LM-35** sensor with an **8051 microcontroller** using an ADC through serial peripheral interfacing to display real-time temperature on an LCD screen
- Wrote **assembly** code for generating voltage waveforms corresponding to input music notes, and subsequently interfaced with an output audio driver circuit

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Design and Simulation of a Multicycle and a Pipelined Processor **[Jan '22 - Apr '22]**

Guide: Prof. Virendra Singh, Electrical Engineering, IIT Bombay

- Coordinated a four-member team to design a **Six-Stage Pipelined processor**, which was optimized for performance using **hazard mitigation** and a Multi-cycle processor with a given modified **RISC ISA**
- Designed a **Lookup Table** for branch prediction and a **feed-forward** logic to increase the throughput
- Implemented the complete design of the two processors and **tested** it on **VHDL** using **Quartus Prime**

Design of Valet Parking Bot **[Jan '23 - Apr '23]**

Guide: Prof. Kavi Arya, Prof. Paritosh Pandya , Computer Science and Engineering, IIT Bombay

- Led a team of 3 to program a bot to traverse test tracks and park itself avoiding any obstacle
- Deigned a PID-based robust line following algorithm using **Heptagon**, a synchronous dataflow language
- Implemented an obstacle avoidance algorithm by interfacing infrared sensors with **ATmega328P**

Digital Logic Design in VHDL | **Digital Circuits Lab** **[Sep '21 - Nov '21]**
Guide: Prof. M.Shojaei Baghini, Electrical Engineering, IIT Bombay

- Designed optimized Combinational and Sequential Circuits using **Structural** and **Behavioural** modelling
- Utilized **Behavioural** modelling to design a **Melay Machine (Finite State Machine)** which iterates over a large string and checks whether a specific string occurred in order or not
- Performed RTL and Gate Level simulations on **Quartus Prime** with a TRACEFILE to verify the design
- Used Krypton Board **(CPLD)** to upload the design and run ScanChain to check the feasibility of the design

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Hand Gesture controlled Self-Balancing Bot | **ITSP** **[Apr '21 - Jul '21]**
Institute Technical Summer Project, ITC | IIT Bombay

- Designed a **PID** controller based two-wheeled self-balancing bot with **Gesture** control for locomotion
- Integrated the robot control program with **Gesture Recognition** python program using **OpenCV**
- Simulated a virtual environment in **Gazebo** using **ROS** and successfully controlled the bot using gestures

Technical Skills

Languages	Python, C++, VHDL, LaTeX, Assembly, Embedded C, Verilog
Softwares & tools	Docker, CUDA, GP-GPU Sim, GEM5, Champsim, Quartus Prime, GNU Radio, NGSpice, Cadence, ROS2, Gazebo, Git, ANSYS HFSS, GHDL, Eagle

Mentorship Experience

Electrical and Communication Subsystem Head **[May '22 - Present]**
Student Satellite Program, IIT Bombay

- Executed a **three-step** recruitment process to shortlist 10 students for the each subsystem from **100+** applicants by evaluating their technical ability, practical approach, and teamwork over 3 weeks
- Mentored **10+** students in the team in learning embedded C programming for **AVR processors**, serial communication protocols for data transfer, **RF PCB design**, and antenna theory

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Mentor, CANSAT | **Student Satellite Program, IIT Bombay** **[Nov '22 - Sep '23]**
Student competition to design a can-sized sub-orbital payload conducted by IN-SPACe, India

- Mentored a team of **5+** students to design a Can-sized payload with active attitude and passive descent control
- Ideated creative techniques for parachute deployment, **2-axis reaction wheel** setup for attitude control and establishing a long-range communication link using high gain ground station and efficient **data packetization**
- Guided the team to efficiently perform testing of on-board processor, sensors, long-range communication link, and live video transmission for a distance of over **1.5KM**

Key Courses

Computer Science	Advanced Topics in Computer Architecture, Advanced Computer Architecture, Microprocessors, Data Structures and Algorithms, , Principles of Data and System Security, Embedded Systems
Digital Design & VLSI	VLSI Design, Algoritmic Design of Digital Systems, Digital Systems
Machine Learning	Image Processing, Programming for Data Science, Intro to Machine Learning
Electrical Engineering	Electronic Design Lab, Communication Networks, Analog Circuits, Electronic Devices, Signal Processing, Communication Systems, Electromagnetic Waves, Control Systems, Power Engineering, Radiating Systems, Electric Drives.

Extracirricular Activities

- Secured **2nd** position among 9 participating teams in **Institute Table Tennis Championship**. *[2023]*
- Secured **1st** position among 9 participating teams in **Institute Triatholon Championship**. *[2022]*
- Stood **3rd** in **Intra-Department Football tournament** among 10 participating teams. *[2022]*
- Stood 2nd among 5 participating teams in **Pluto Fiesta** football event, an annual event of Hostel-9 *[2022]*
- Participated in the **Glider** making event conducted by Aero-modelling Club, IIT Bombay *[2021]*
- Attended a Satellite tracking session conducted by Ham Radio Club | IITB, and tracked **NOAA-15** and **NOAA-18** satellites to receive weather images using **WebSDR** *[2021]*
- Complete a year-long training under **National Sports Organization**(NSO), IIT Bombay *[2021]*